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EXAMINER	
SANTIAGO, MARICELI	

ART UNIT	PAPER NUMBER
2879	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTO-PAT-Email@rfem.com

Office Action Summary	Application No.	Applicant(s)	
	10/542,378	LEE ET AL.	
	Examiner	Art Unit	
	Mariceli Santiago	2879	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/17/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Receipt of the Amendment, filed on November 17, 2008, is acknowledged.

Cancellation of claim 2 has been entered.

Claims 1 and 3-19 are pending in the instant application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 and 3-6 are rejected under 35 U.S.C. 103(a) as being obvious over Marcus et al. (US 5,100,355) in view of Borel et al. (US 4,940,916).

Regarding claim 1, Marcus discloses a field emission display (FED) with an integrated triode structure (Fig. 8), comprising a substrate (26), cathode layer (24) positioned on the substrate, a gate insulating layer (36), which is positioned on the cathode substrate and has a plurality of sub-microholes arranged in a regular pattern, a gate electrode layer (40), which is positioned on the gate insulating layer and has a plurality of sub-microholes arranged in the substantially same pattern as that of the sub-microholes in the gate insulating layer, an anode insulating layer (38), which is positioned on the gate electrode layer and has a plurality of sub-microholes arranged in the substantially same pattern as that of the sub-microholes in the gate insulating layer, emitters (30, 32), which are positioned in wells defined by the sub-microholes in the gate insulating layer, the gate electrode layer and the anode insulating layer, and the emitters (28) being adhered to the cathode layer, a phosphor layer (42) positioned on the anode

insulating layer, and an anode layer (44) positioned on the phosphor layer. Marcus fails to exemplify the limitation of a resistive layer which is positioned between the cathode layer and the gate insulating layer. Borel discloses a field emission display with an integrated triode structure (Fig. 4), comprising a substrate (2), cathode layer (22) positioned on the substrate, a gate insulating layer (8), which is positioned on the cathode substrate and has a plurality of sub-microholes arranged in a regular pattern, a gate electrode layer (10), which is positioned on the gate insulating layer and has a plurality of sub-microholes arranged in the substantially same pattern as that of the sub-microholes in the gate insulating layer, and a resistive layer (24) which is positioned between the cathode layer (22) and the gate insulating layer (8), the resistive layer is such positioned so as to enhance emission uniformity, limit the overcurrent and perform heat dissipation in case of shortcircuits. Thus, it would have been obvious at the time the invention was made to a person having ordinary skills in the art to incorporate the resistive layer disclosed by Borle in the device of Marcus in order to enhance emission uniformity, limit the overcurrent and perform heat dissipation in case of shortcircuits.

Regarding claim 3, Marcus fails to exemplify the limitation of the wells have a diameter of 4 to 500 nm. It has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide wells having a diameter of 4 to 500 nm, since optimization of workable ranges is considered within the skill of the art.

Regarding claim 4, Marcus discloses a field emission display wherein the thickness of the anode insulating layer is in the range of 100nm and 10μm (Column 5, lines 37-38).

Regarding claim 5, Marcus discloses a field emission display wherein the anode layer hermetically seals discharge spaces defined by the wells (Fig. 8).

Regarding claim 6, Marcus discloses a field emission display further comprising a front plate (46) which is positioned on the anode layer.

Claims 1, 3-5 and 7-19 are rejected under 35 U.S.C. 103(a) as being obvious over Lee et al. (WO 2004/012218) in view of Marcus et al. (US 5,100,355).

The applied reference has common inventors with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Regarding claim 1, Lee discloses a field emission display (FED) with an integrated triode structure, comprising a substrate (200), cathode layer (202) positioned on the substrate, a gate insulating layer (206), which is positioned on the cathode substrate and has a plurality of sub-microholes arranged in a regular pattern, a resistive layer which is positioned between the cathode layer and the gate insulating layer, a gate electrode layer (208), which is positioned on the gate insulating layer and has a plurality of sub-microholes arranged in the substantially same pattern as that of the sub-microholes in the gate insulating layer, an anode insulating layer (38), which is positioned on the gate electrode layer and has a plurality of sub-microholes

arranged in the substantially same pattern as that of the sub-microholes in the gate insulating layer, emitters (218), which are positioned in wells defined by the sub-microholes in the gate insulating layer, the gate electrode layer and the anode insulating layer, and the emitters (28) being adhered to the cathode layer, and an anode layer (220) positioned on the anode insulating layer.

Lee teaches the use of the field emission device for display purposes, but fails to exemplify providing a phosphor layer positioned between the anode insulating layer and the anode layer. However, in the same field of endeavor, Marcus discloses a field emission display provided with a phosphor layer between the anode insulating layer and the anode layer in order to display an image upon excitation of the phosphor layer by the field emission. Thus, it would have been obvious at the time the invention was made to a person having ordinary skills in the art to incorporate the phosphor layer disclosed by Marcus in the device of Lee in order to provide image display upon excitation of the phosphor by the field emission.

Regarding claim 3, Lee fails to exemplify the limitation of the wells have a diameter of 4 to 500 nm. It has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide wells having a diameter of 4 to 500 nm, since optimization of workable ranges is considered within the skill of the art.

Regarding claim 4, Lee discloses a field emission display wherein the thickness of the anode insulating layer is in the range of 100nm and 10μm (Page 11, lines 2-4).

Regarding claim 5, Lee discloses a field emission display wherein the anode layer hermetically seals discharge spaces defined by the wells (Fig. 2F).

Regarding claim 7, Lee discloses a method for manufacturing a FED with an integrated triode structure, the method comprising: (a) forming, on a substrate, a cathode layer, a gate insulating layer, a gate electrode layer, and an aluminum layer, in order; (b) converting the aluminum layer to an alumina layer using anodic oxidation, until the alumina layer has sub-microholes in a regular arrangement pattern and a barrier layer remained at the lower part of the sub-microholes; (c) extending the depth of the sub-microholes in the alumina layer to the surface of the cathode layer, (d) forming emitters in the sub-microholes, the emitters being adhered to the cathode layer; and (f) forming an anode layer on the alumina layer under vacuum atmosphere.

Lee teaches the use of the field emission device for display purposes, but fails to exemplify the step of forming a phosphor layer on the alumina layer. However, in the same field of endeavor, Marcus discloses a field emission display provided with a phosphor layer between the anode insulating layer and the anode layer in order to display an image upon excitation of the phosphor layer by the field emission. Thus, it would have been obvious at the time the invention was made to a person having ordinary skills in the art to incorporate the phosphor layer disclosed by Marcus in the method of Lee in order to provide image display upon excitation of the phosphor by the field emission.

Regarding claim 8, Lee discloses a method wherein step (a) further comprises forming a resistive layer on the cathode layer, in step (c), the depth of the sub-microholes is extended to the surface of the resistive layer and, and in step (d), the emitters are adhered to the resistive layer.

Regarding claim 9, Lee discloses a method wherein in step (b), the anodic oxidation comprises applying a positive voltage to the aluminum layer in aqueous solution of acidic electrolyte.

Regarding claim 10, Lee discloses a method wherein the acidic electrolyte is selected from the group consisting of oxalic acid, sulfuric acid, sulfonic acid, phosphoric acid, and chromic acid.

Regarding claim 11, Lee discloses a method wherein in step (b), the diameter of the sub-microholes is in the range of 4 to 500 nm.

Regarding claim 12, Lee discloses a method wherein step (c) is carried out using ion milling, dry etching, wet etching, or anodic oxidation.

Regarding claim 13, the combined references to Lee-Marcus is silent in regards to wherein step (e), a phosphor is applied to the alumina layer using e-beam evaporation, thermal evaporation, sputtering, low-pressure chemical vapor deposition, sol-gel method, electroplating, or electroless plating. However, one skilled in the art would reasonable contemplate deposition of the phosphor layer by means of one of the claimed techniques as an obvious matter of design engineering since any of such processes are readily available and recognized in the art. Thus, it would have been obvious at the time the invention was made to a person having ordinary skills in the art to use any of the deposition process readily available and art recognized for depositing the phosphor layer disclosed by Marcus, since such modification would be considered an obvious matter of design engineering.

Regarding claim 14, Lee discloses a method wherein the method further comprises increasing the diameter of the sub-microholes in the alumina layer by post-chemical treatment after step (b).

Regarding claim 15, Lee discloses a method for manufacturing a FED with an integrated triode structure, the method comprising: (a) forming, on a substrate, a cathode layer, a gate insulating layer, a gate electrode layer, an anode insulating layer and an aluminum layer, in order; (b) converting the aluminum layer to an alumina layer using anodic oxidation, until the

alumina layer has sub-microholes in a regular arrangement pattern and a barrier layer remained at the lower part of the sub-microholes; (c) extending the depth of the sub-microholes in the alumina layer to the surface of the cathode layer; (c1) removing the alumina layers; (d) forming emitters in the sub-microholes, the emitters being adhered to the cathode layer; and (f) forming an anode layer on the anode insulating layer under vacuum atmosphere.

Lee teaches the use of the field emission device for display purposes, but fails to exemplify the step of forming a phosphor layer on the alumina layer. However, in the same field of endeavor, Marcus discloses a field emission display provided with a phosphor layer between the anode insulating layer and the anode layer in order to display an image upon excitation of the phosphor layer by the field emission. Thus, it would have been obvious at the time the invention was made to a person having ordinary skills in the art to incorporate the phosphor layer disclosed by Marcus in the method of Lee in order to provide image display upon excitation of the phosphor by the field emission.

Regarding claim 16, Lee discloses a method, wherein the anode insulation layer isformed of SiO_2.

Regarding claim 17, Lee discloses a method, wherein step (c1) is carried out by dipping it in a solution of phosphoric acid or a mixed solution of phosphoric acid and chromic acid.

Regarding claim 18, Lee discloses a method, wherein step (a) further comprises forming a resistive layer on the cathode layer, in step (c), the depth of the sub-microholes is extended to the surface of the resistive layer and, and in step (d), the emitters are adhered to the resistive layer.

Regarding claim 19, Lee discloses a method, wherein the method further comprises increasing the diameter of the sub-microholes in the alumina layer by post-chemical treatment after step (b).

Response to Arguments

Applicant's arguments with respect to claims 1 and 3-6 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments filed November 17, 2008, in regards to the rejection of claims 1, 3-5 and 7-19 under 35 U.S.C. 103(a) as being obvious over Lee et al. (WO 2004/012218) in view of Marcus et al. (US 5,100,355), have been fully considered but they are not persuasive.

Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15. Perfecting of the claim for priority requires an official English translation of the foreign priority documents, it does not rely merely in the submission of the certified priority documents.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mariceli Santiago whose telephone number is (571) 272-2464. The examiner can normally be reached on Monday-Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel, can be reached on (571) 272-2457. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Mariceli Santiago/
Primary Examiner, Art Unit 2879